ĐẠI HỌC QUỐC GIA TP.HỒ CHÍ MINH
TRƯỜNG ĐẠI HỌC BÁCH KHOA
KHOA ĐIỆN-ĐIỆN TỬ
BỘ MÔN KỸ THUẬT ĐIỆN TỬ


# ASIC AND IP CORE DESIGN

## Chapter 0: Course Introduction

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# Course Information

- Instructor
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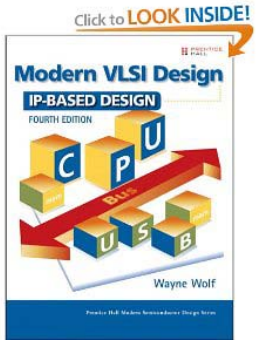
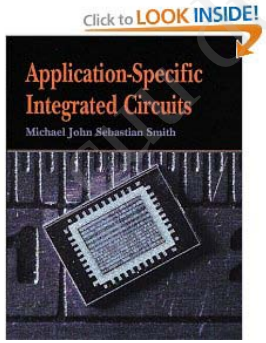
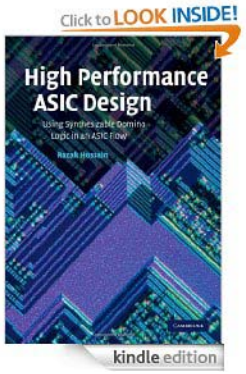
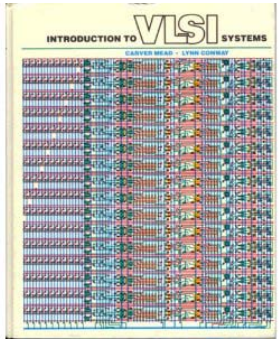
# Textbooks

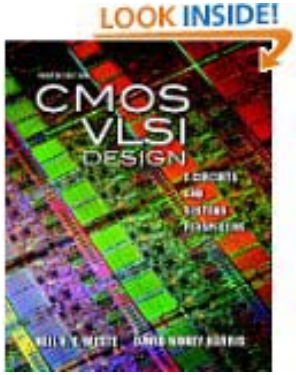
1. **Wayne Wolf,** *Modern VLSI Design – IP-Based Design, Prentice-Hall, 4th edition, 2008*
2. **Michael Smith,** *Application-Specific Integrated Circuits*, Addison Wesley, 1997
3. **Razak Hossain,** *High Performance ASIC Design,* Cambridge, 2008.
4. **Mead C. and Conway L.,** *Introduction to VLSI Systems, Addison Wiley*, 2005.
5. **Neil Weste and David Harris,** *CMOS VLSI Design A Circuits and Systems Perspective, Addison Wesley, 2010*





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# Course Description

- Provide students general and detail knowledge of chip design on ASIC and FPGA
- Master the Verilog (or VHDL) language for hardware programming
- Master the necessary tools for ASIC chip design

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# Course Outcomes

- Skills to use the Synopsys tools for simulation, verification and layout design.
- Skills to design a IC with Verilog language from a defined specifications.
- Skills to design and optimize architecture of the design
- Skills to use the Modelsim (VCS or NCSim) for IC verification.
- Skills to write the scripts to automate the testbench (testcase) during the verification process.
- Skills to check, compile & synthesize the IC design toward ASIC technology (Leda, Compiler).
- Skills to verify the timing constraint during IC physical design (PrimeTime).
- Skills to verify the layout with tools: Hercule & Astro.

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# Syllabus

| Chapter | Content | Hours |
|---|---|---|
| 1 | **Introduction: ASIC chip design & IP design**<br>1.1 ASIC and FPGA-based chip design flow<br>1.2 IP design<br>1.3 ASIC chip: analog versus digital | 3 |
| 2 | **IC Fabrication**<br>2.1 Fabrication process<br>2.2 Transistors<br>2.3 Layout and design tools | 6 |
| 3 | **Architecture design**<br>3.1 Design Entry<br>3.2 Design Constraints<br>3.3 Hardware Description Language<br>3.3 Design Synthesis | 6 |

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# Syllabus

| Chapter | Content | Hours |
|---|---|---|
| 4 | **Verification process**<br>4.1 Test environment<br>4.2 Testbench<br>4.3 Formal verification<br>4.4 Boundary-scan test | 6 |
| 5 | **Physical design**<br>5.1 System partitioning<br>5.2 Floorplanning and placement<br>5.3 Routing | 6 |

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# Grading

- Assignment: 20%
- Final exam: 50%
- Project: 30%
  - 1 - 2 students for one group
  - Select project's topic at **week 1-2**
  - Submit project at **week 13**

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# Schedule

| Week | Lecture |
|---|---|
| 1 | Chapter 0 |
| 2 | Chapter 1 |
| 3 | Chapter 2 |
| 4 | Chapter 2 |
| 5 | Chapter 3 |
| 6 | Chapter 3 |
| 7 | Chapter 4 |
| 8 | Midterm |
| 9 | Midterm |

| Week | Lecture |
|---|---|
| 10 | Chapter 4 |
| 11 | Chapter 5 |
| 12 | Chapter 5 |
| 13 | Present project |
| 14 | Present project |
| 15 | Present project |
| 16 | Present project |
| 17 | Extra |
| 18-19 | Final exam |

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# Course Preparation

- Textbooks:
  - download at least 3 required textbooks
- Software tools:
  - ModelSim, Quartus II
  - Synopsys
  - Virtuoso
- Programming knowledge:
  - VHDL/Verilog

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# Project's Topics

1. Viterbi decoder
2. Color correction IP core
3. Color interpolation IP core
4. Edge detection using Prewitt and Sobel operator
5. SDR SDRAM controller
6. DDR SDRAM controller
7. AHB interface
8. AES encryption
9. DES encryption
10. DCT transform
11. Wavelet transform
12. Contourlet transform

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# Project's requirements

- Report in MS Word
- Simulate the design in Modelsim or VCS
- Verify the design on FPGA
  - Altera DE2 kit
- Synthesize by Synopsys tool
- Present the design in class (option, bonus score)

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